Fig. 1

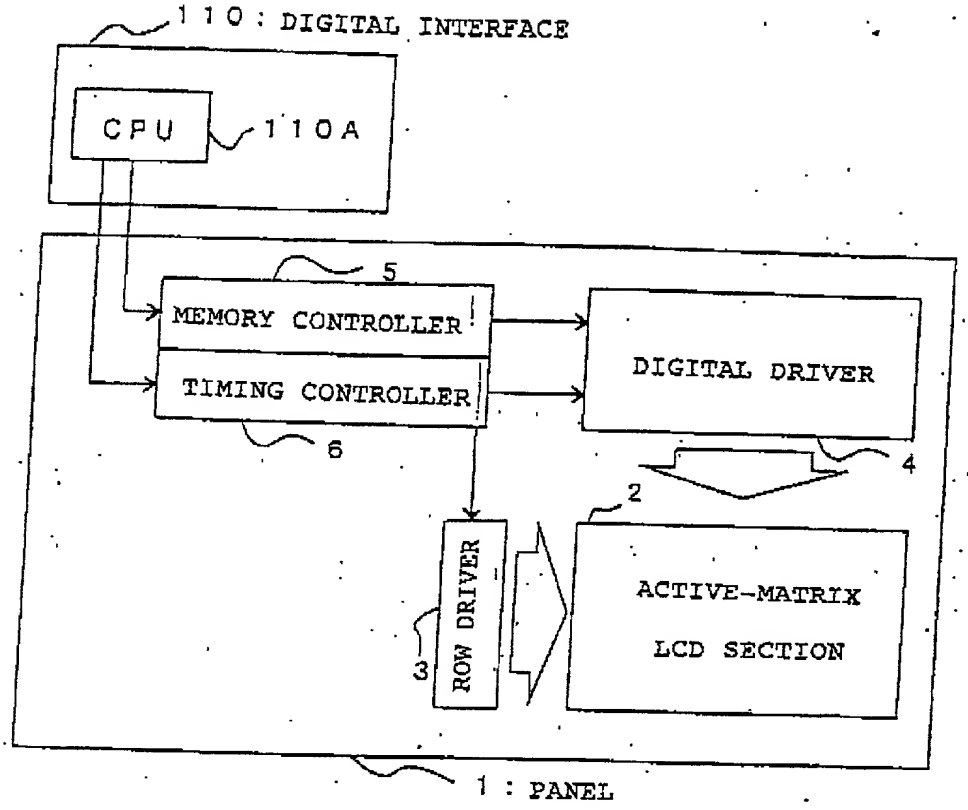

110 : DIGITAL INTERFACE
CPU
110A
5
MEMORY CONTROLLER
TIMING CONTROLLER
6
DIGITAL DRIVER
4
2
ROW DRIVER
3
ACTIVE-MATRIX
LCD SECTION
1 : PANEL

Fig. 2

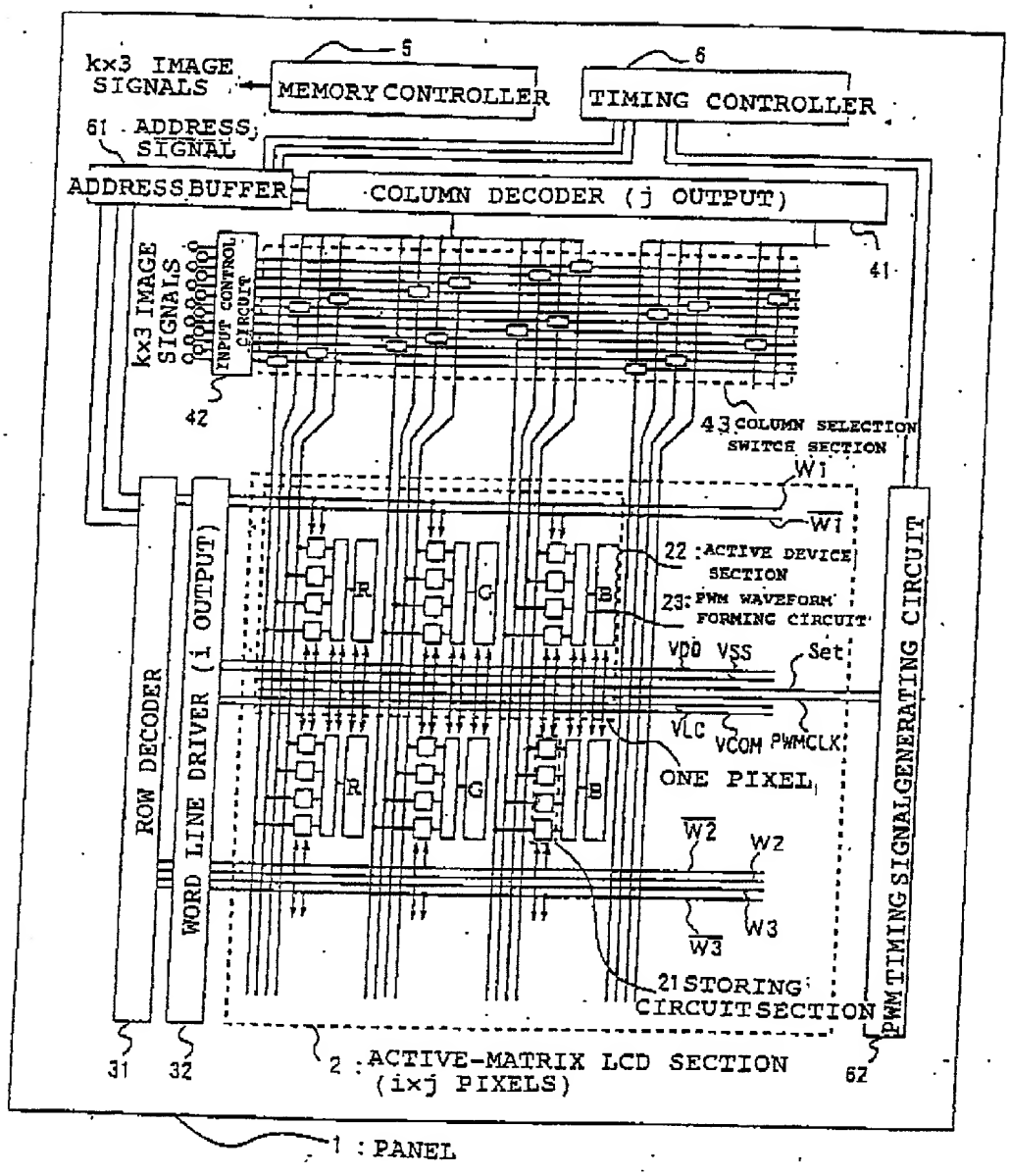

kx3 IMAGE SIGNALS
5
MEMORY CONTROLLER
6
TIMING CONTROLLER
61 ADDRESS SIGNAL
ADDRESS BUFFER
COLUMN DECODER (j OUTPUT)
41
kx3 IMAGE SIGNALS
INPUT CONTROL CIRCUIT
42
43 COLUMN SELECTION SWITCH SECTION
W1
W1
22 : ACTIVE DEVICE SECTION
23: PWM WAVEFORM FORMING CIRCUIT
R
G
B
VDD VSS
Set
VLC
VCOM
PWMCLK
ONE PIXEL
W2
W2
W3
W3
21 STORING CIRCUIT SECTION
ROW DECODER
WORD LINE DRIVER (i OUTPUT)
PWM TIMING SIGNAL GENERATING CIRCUIT
31
32
2 : ACTIVE-MATRIX LCD SECTION (ixj PIXELS)
62
1 : PANEL

Fig. 3

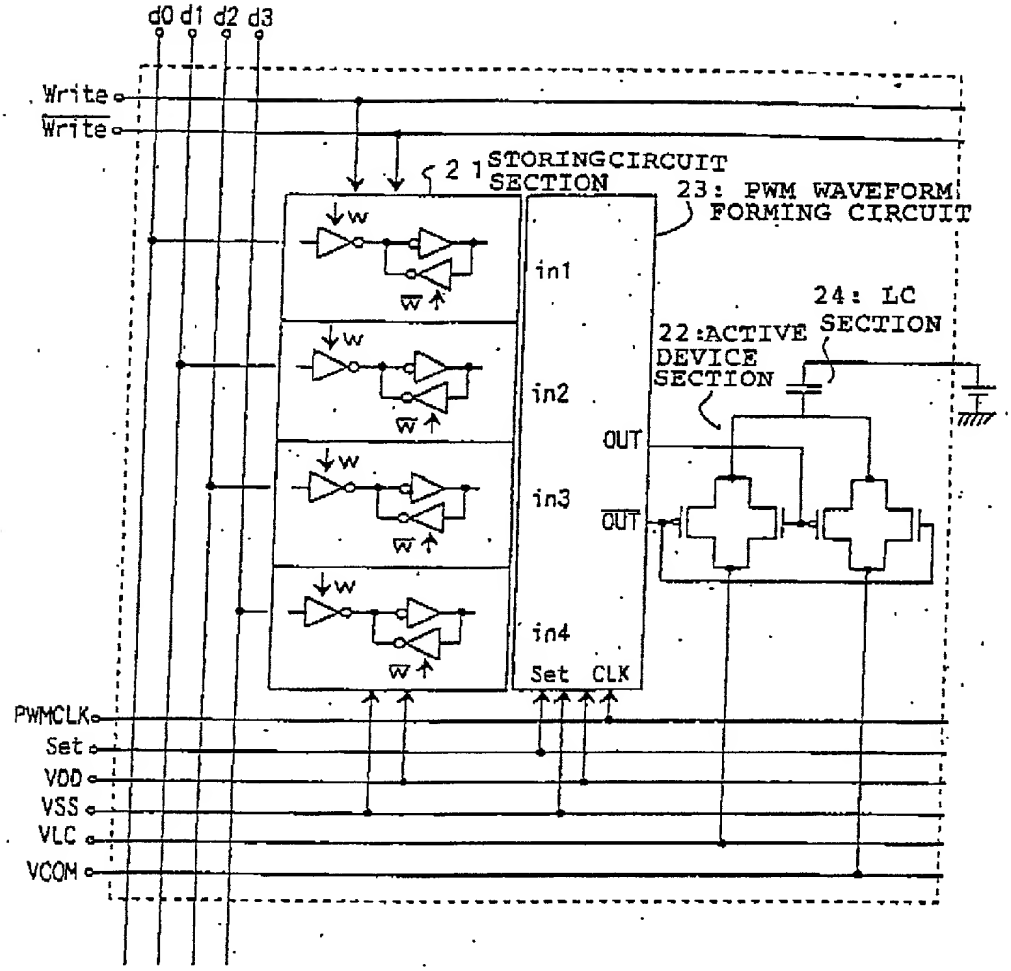

d0 d1 d2 d3
Write
Write
21 STORING CIRCUIT SECTION
23: PWM WAVEFORM FORMING CIRCUIT
24: LC SECTION
22: ACTIVE DEVICE SECTION
w
in1
in2
in3
in4
OUT
OUT
Set
CLK
PWMCLK
Set
VDD
VSS
VLC
VCOM

Fig. 4

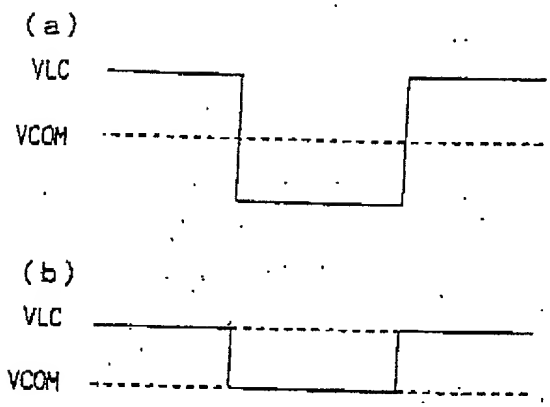


Fig. 5

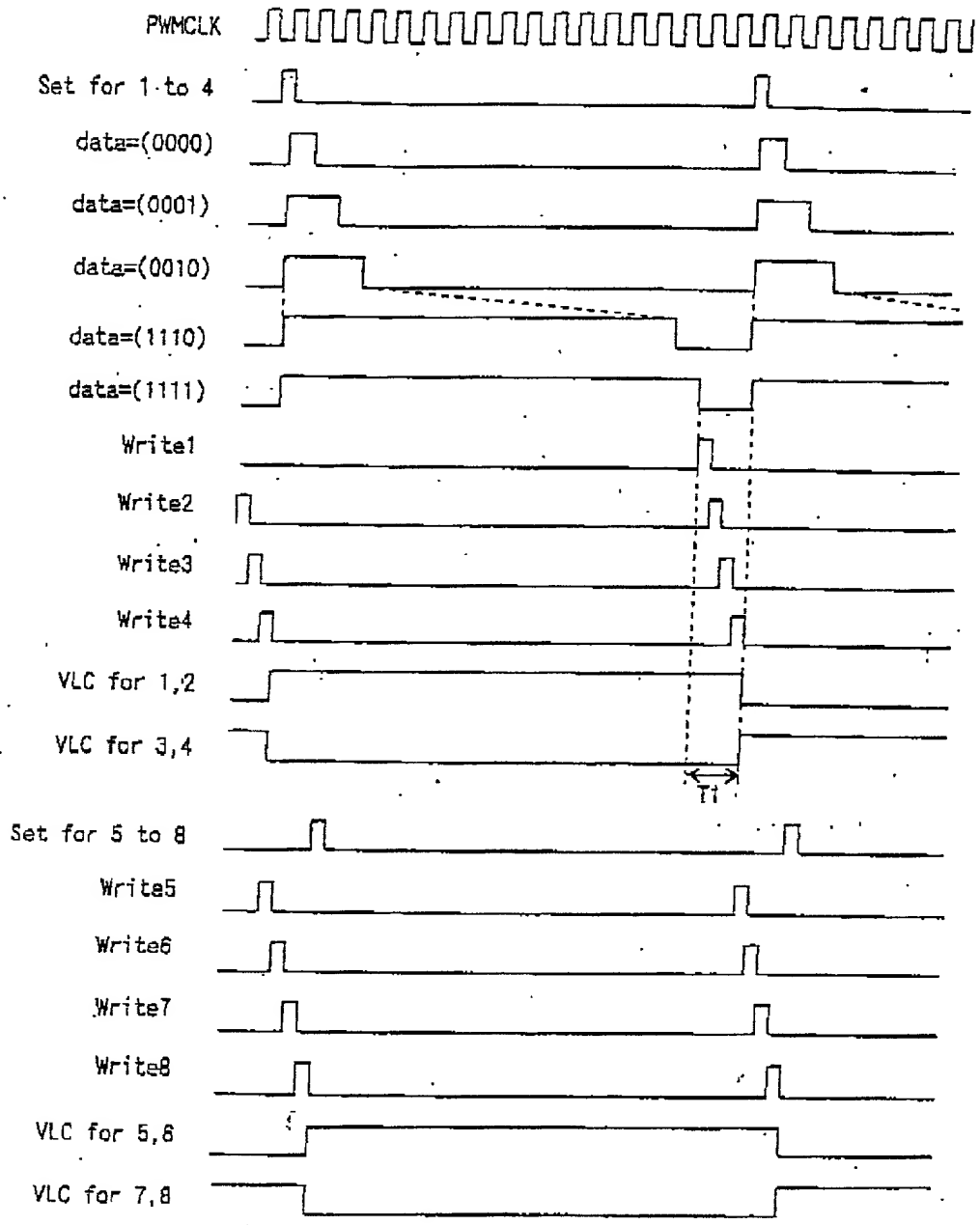

PWMCLK
Set for 1 to 4
data=(0000)
data=(0001)
data=(0010)
data=(1110)
data=(1111)
Write1
Write2
Write3
Write4
VLC for 1,2
VLC for 3,4
T1
Set for 5 to 8
Write5
Write6
Write7
Write8
VLC for 5,6
VLC for 7,8

Fig. 6

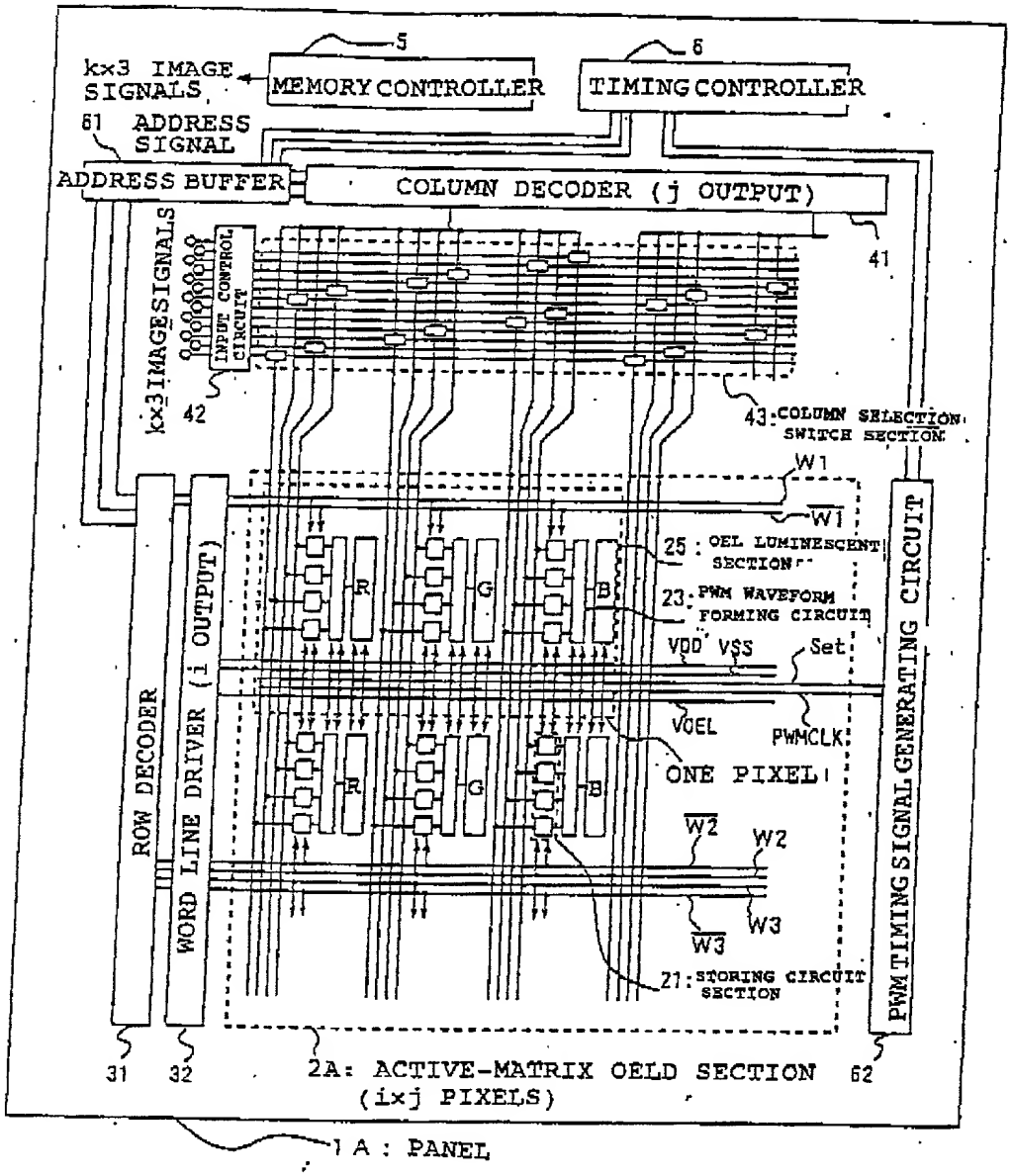

5
6
k×3 IMAGE SIGNALS
MEMORY CONTROLLER
TIMING CONTROLLER
61 ADDRESS SIGNAL
ADDRESS BUFFER
COLUMN DECODER (j OUTPUT)
41
k×3 IMAGE SIGNALS
INPUT CONTROL CIRCUIT
42
43: COLUMN SELECTION SWITCH SECTION
W1
W1
25: OEL LUMINESCENT SECTION
23: PWM WAVEFORM FORMING CIRCUIT
VDD VSS
Set
VOEL
PWMCLK
ONE PIXEL
R
G
B
W2
W2
W3
W3
21: STORING CIRCUIT SECTION
ROW DECODER
WORD LINE DRIVER (i OUTPUT)
PWM TIMING SIGNAL GENERATING CIRCUIT
31
32
2A: ACTIVE-MATRIX OELD SECTION (i×j PIXELS)
62
1A: PANEL

Fig. 7

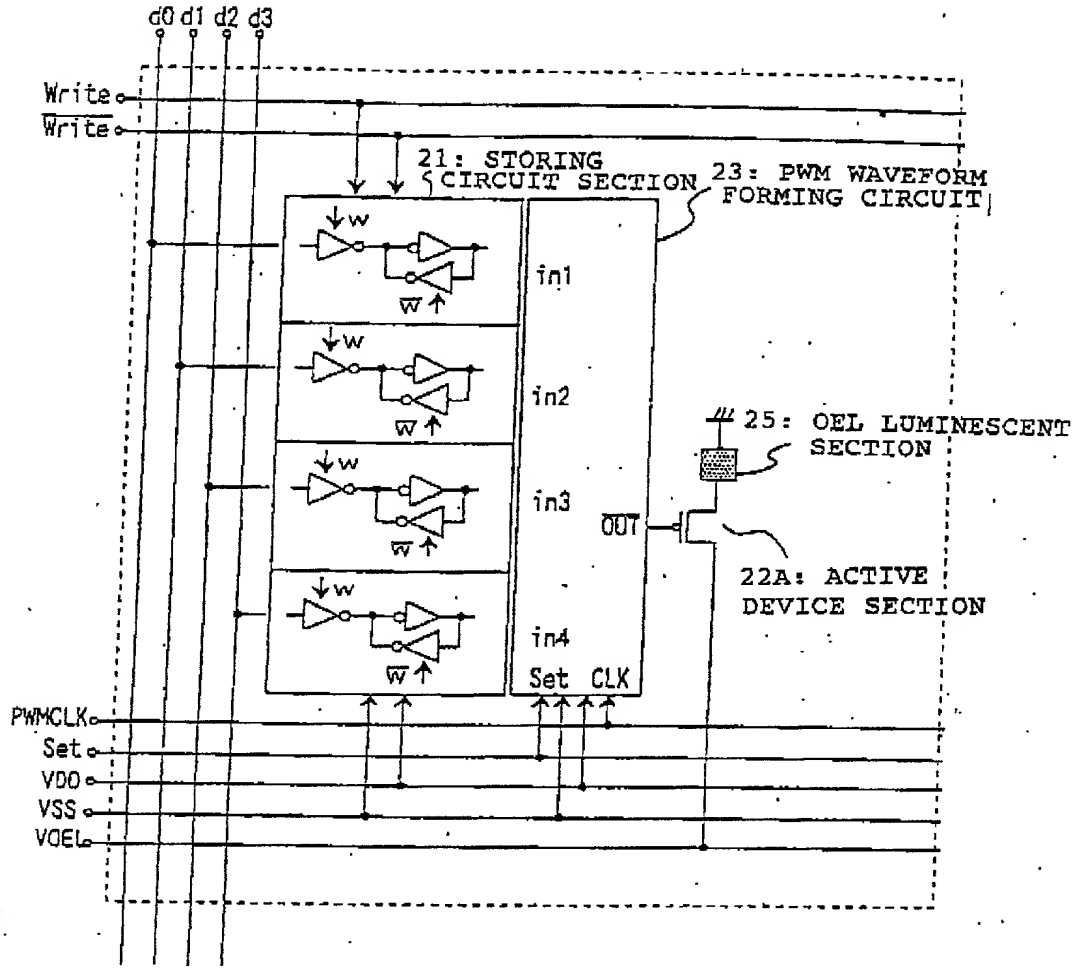

d0 d1 d2 d3
Write
Write
21: STORING CIRCUIT SECTION
23: PWM WAVEFORM FORMING CIRCUIT
w
in1
in2
in3
in4
Set CLK
OUT
25: OEL LUMINESCENT SECTION
22A: ACTIVE DEVICE SECTION
PWMCLK
Set
VDD
VSS
VOEL

Fig. 8

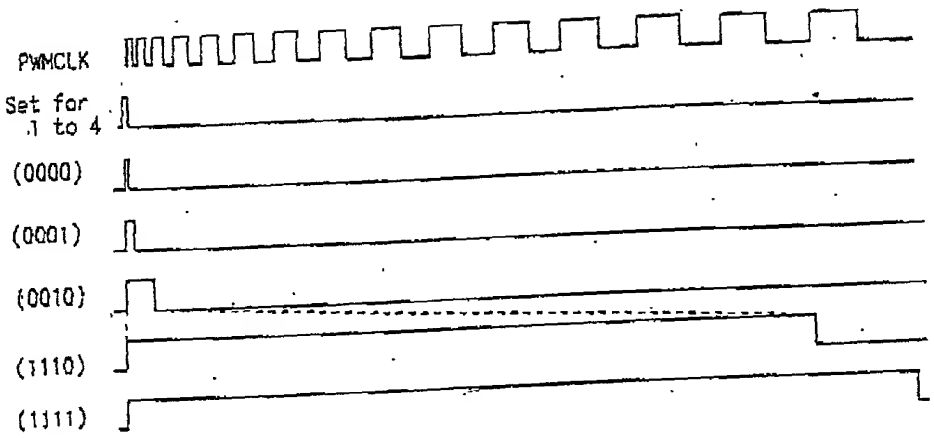


Fig. 9

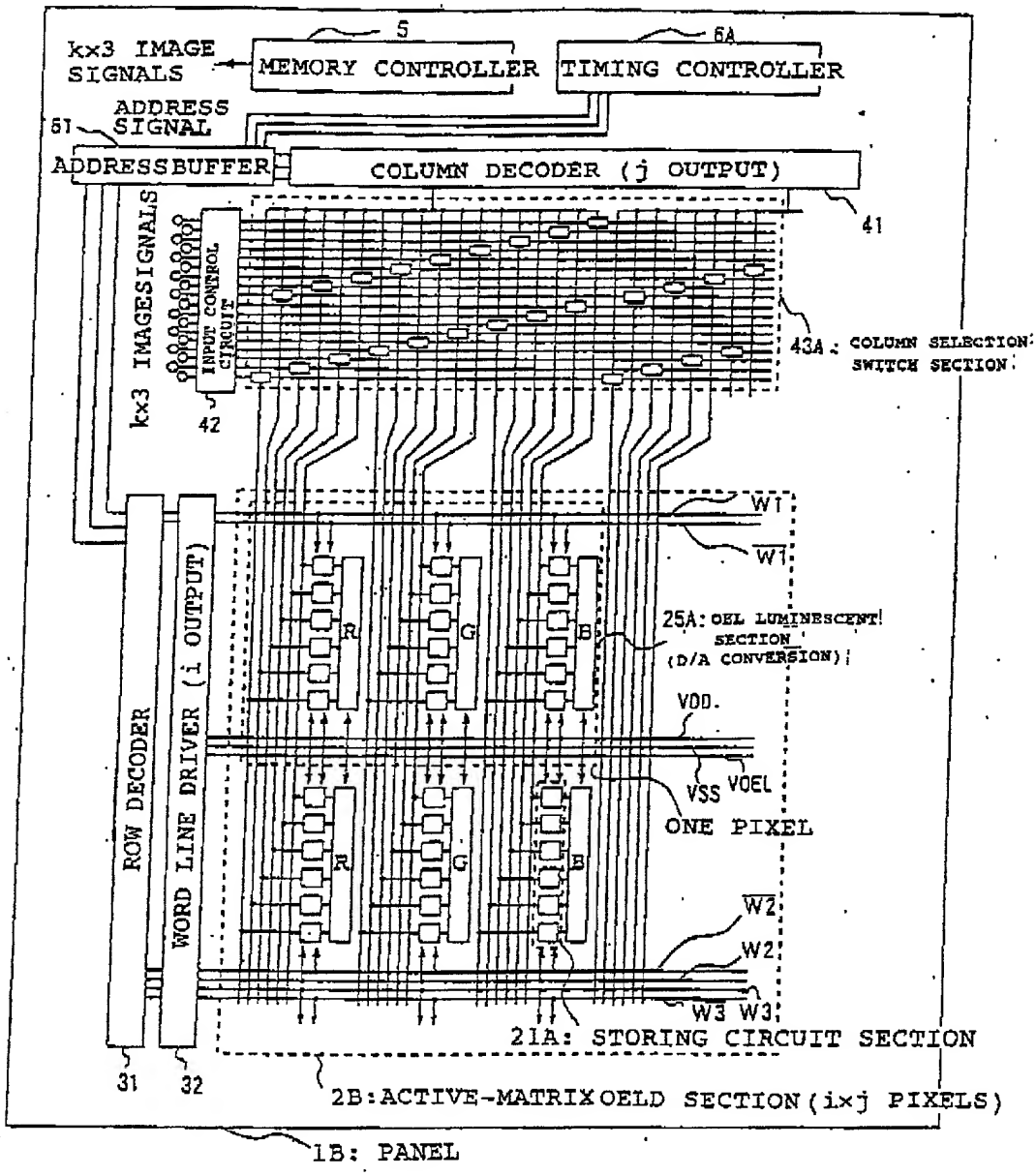

kx3 IMAGE SIGNALS
5
MEMORY CONTROLLER
6A
TIMING CONTROLLER
ADDRESS SIGNAL
51
ADDRESSBUFFER
COLUMN DECODER (j OUTPUT)
41
kx3 IMAGESIGNALS
INPUT CONTROL CIRCUIT
42
43A: COLUMN SELECTION SWITCH SECTION
W1
W1
R
G
B
25A: OEL LUMINESCENT SECTION (D/A CONVERSION)
VDD
VSS
VOEL
ONE PIXEL
W2
W2
W3 W3
21A: STORING CIRCUIT SECTION
ROW DECODER
WORD LINE DRIVER (i OUTPUT)
31
32
2B:ACTIVE-MATRIXOELD SECTION(i×j PIXELS)
1B: PANEL

Fig. 10

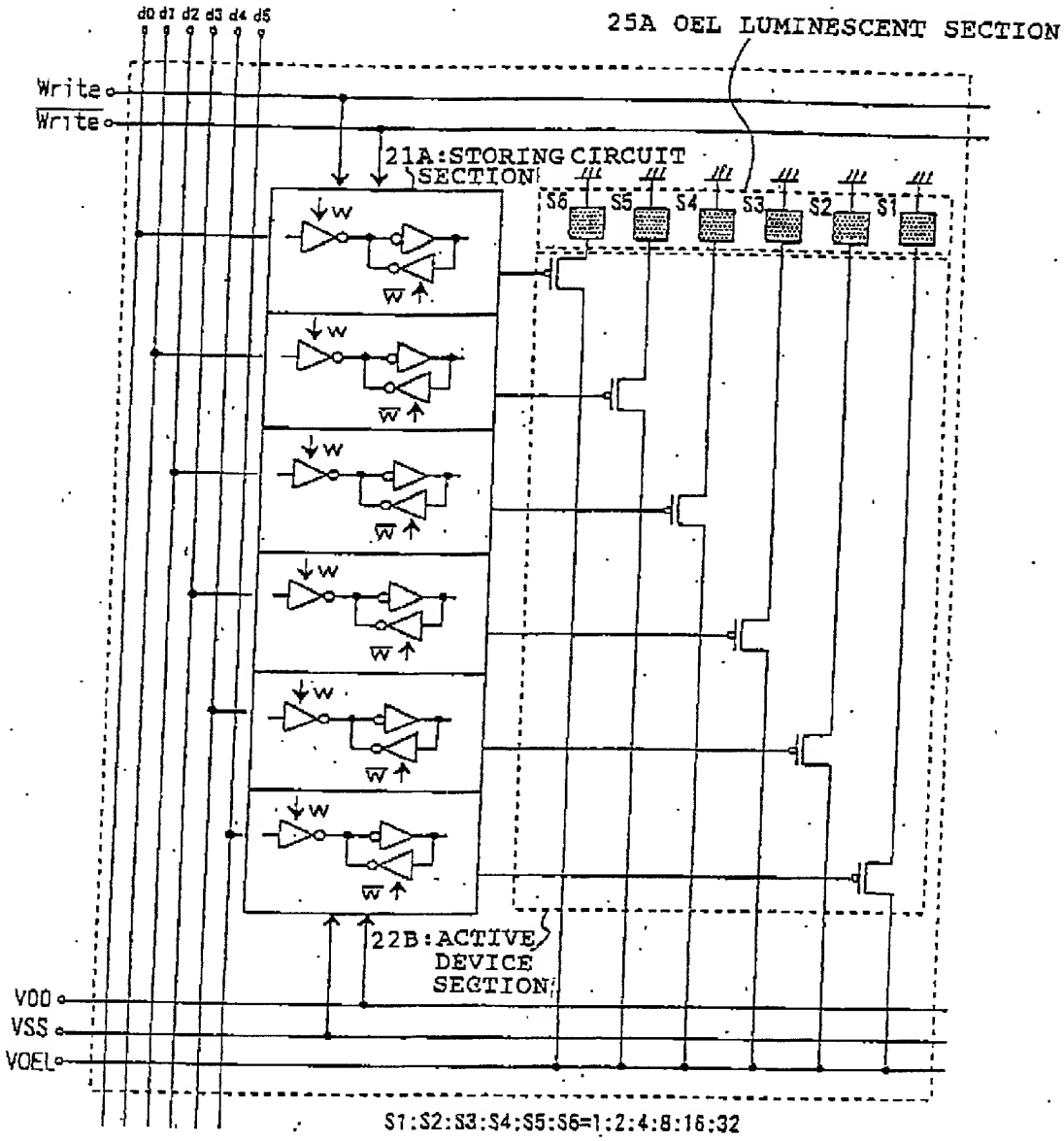

d0 d1 d2 d3 d4 d5
25A OEL LUMINESCENT SECTION
Write
Write
21A:STORING CIRCUIT SECTION
S6 S5 S4 S3 S2 S1
22B:ACTIVE DEVICE SECTION
VDD
VSS
VOEL
S1:S2:S3:S4:S5:S6=1:2:4:8:16:32

Fig. 11

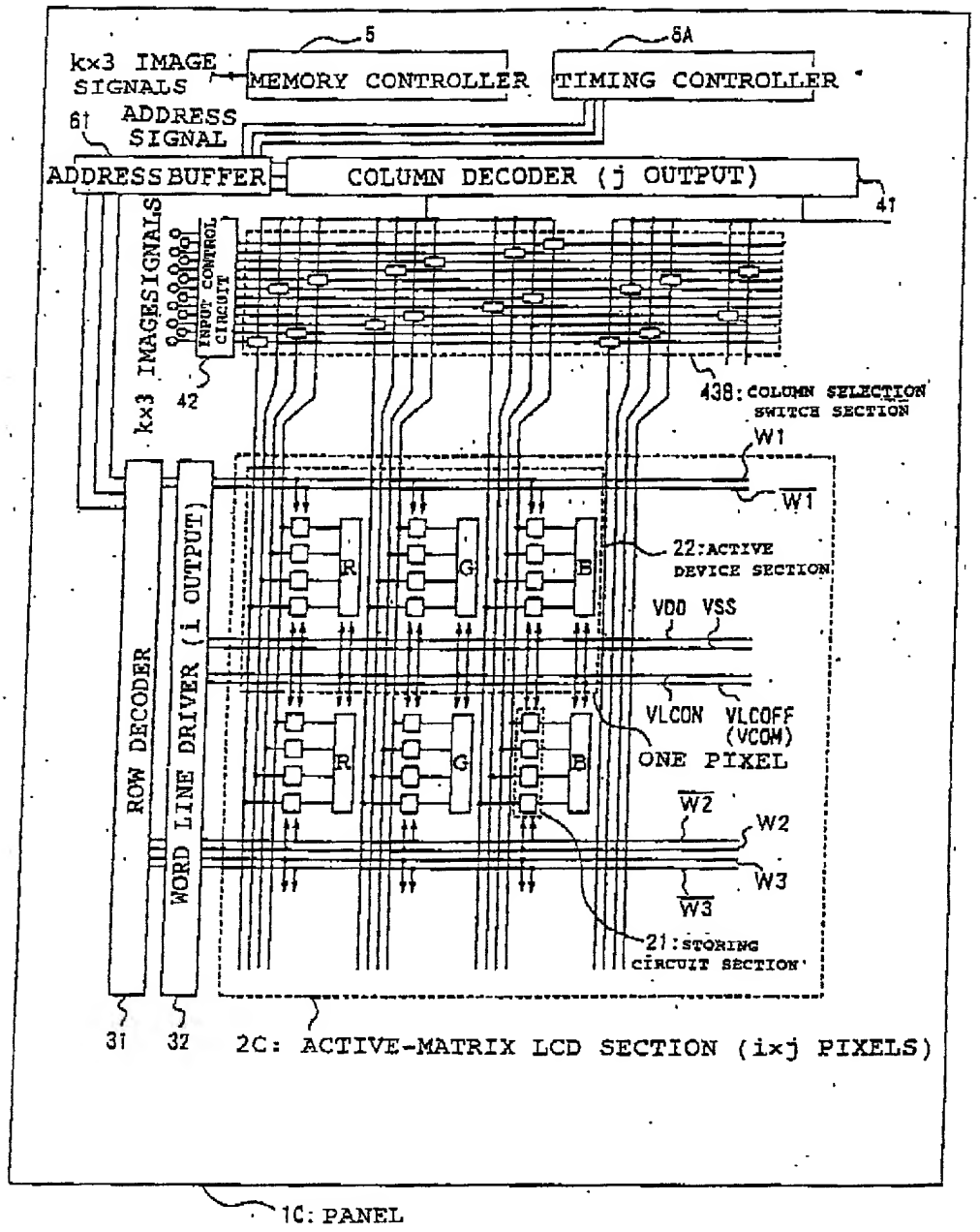

5
5A
k×3 IMAGE SIGNALS
MEMORY CONTROLLER
TIMING CONTROLLER
6
ADDRESS SIGNAL
ADDRESS BUFFER
COLUMN DECODER (j OUTPUT)
41
k×3 IMAGE SIGNALS
INPUT CONTROL CIRCUIT
42
438: COLUMN SELECTION SWITCH SECTION
W1
W1
22: ACTIVE DEVICE SECTION
R
G
B
VDD VSS
VLCON
VLCOFF (VCOM)
ONE PIXEL
W2
W2
W3
W3
21: STORING CIRCUIT SECTION
ROW DECODER
WORD LINE DRIVER (i OUTPUT)
31
32
2C: ACTIVE-MATRIX LCD SECTION (i×j PIXELS)
1C: PANEL

Fig. 12

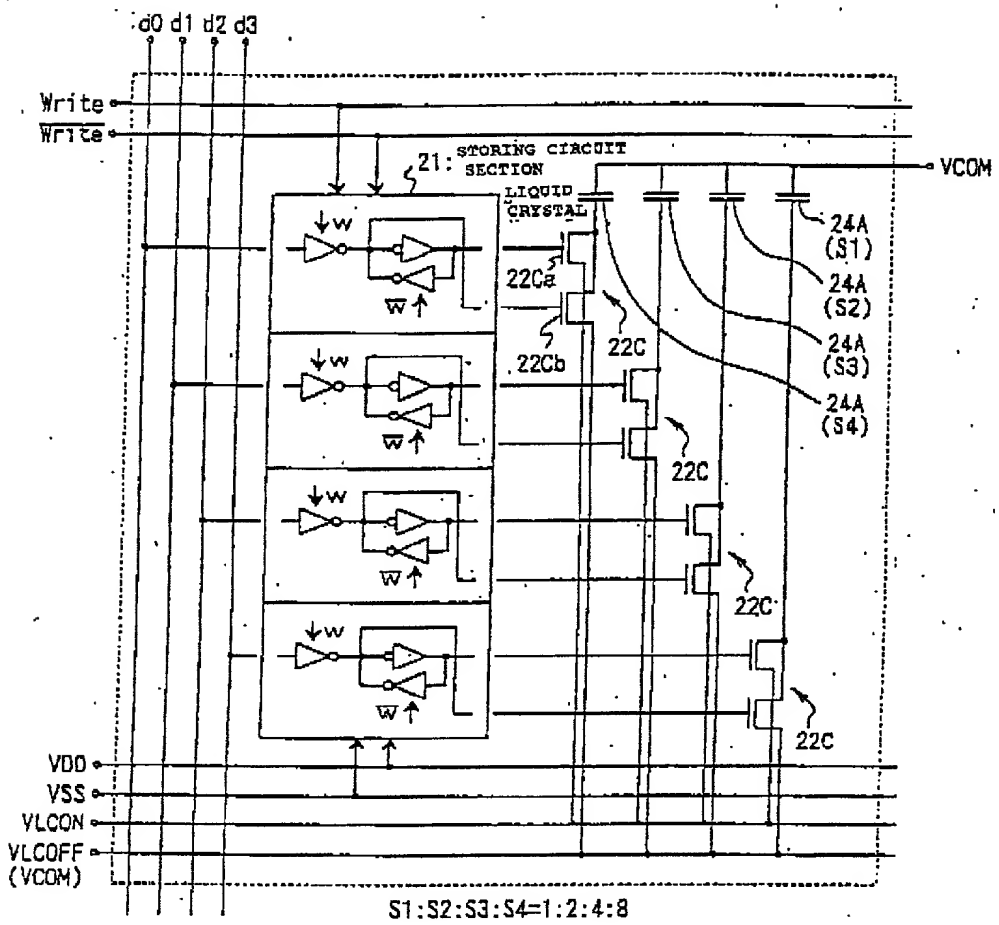

d0 d1 d2 d3
Write
Write
21: STORING CIRCUIT SECTION
LIQUID CRYSTAL
VCOM
24A (S1)
24A (S2)
24A (S3)
24A (S4)
22Ca
22Cb
22C
VDD
VSS
VLCON
VLCOFF (VCOM)
S1:S2:S3:S4=1:2:4:8

Fig. 13

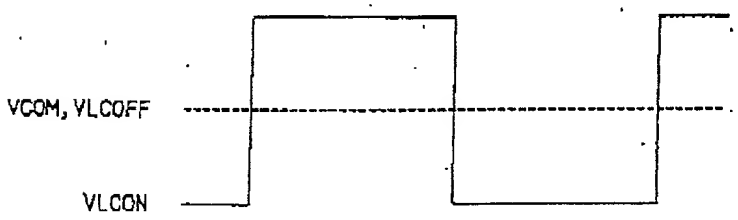

VCOM, VLCOFF
VLCON

Fig. 14

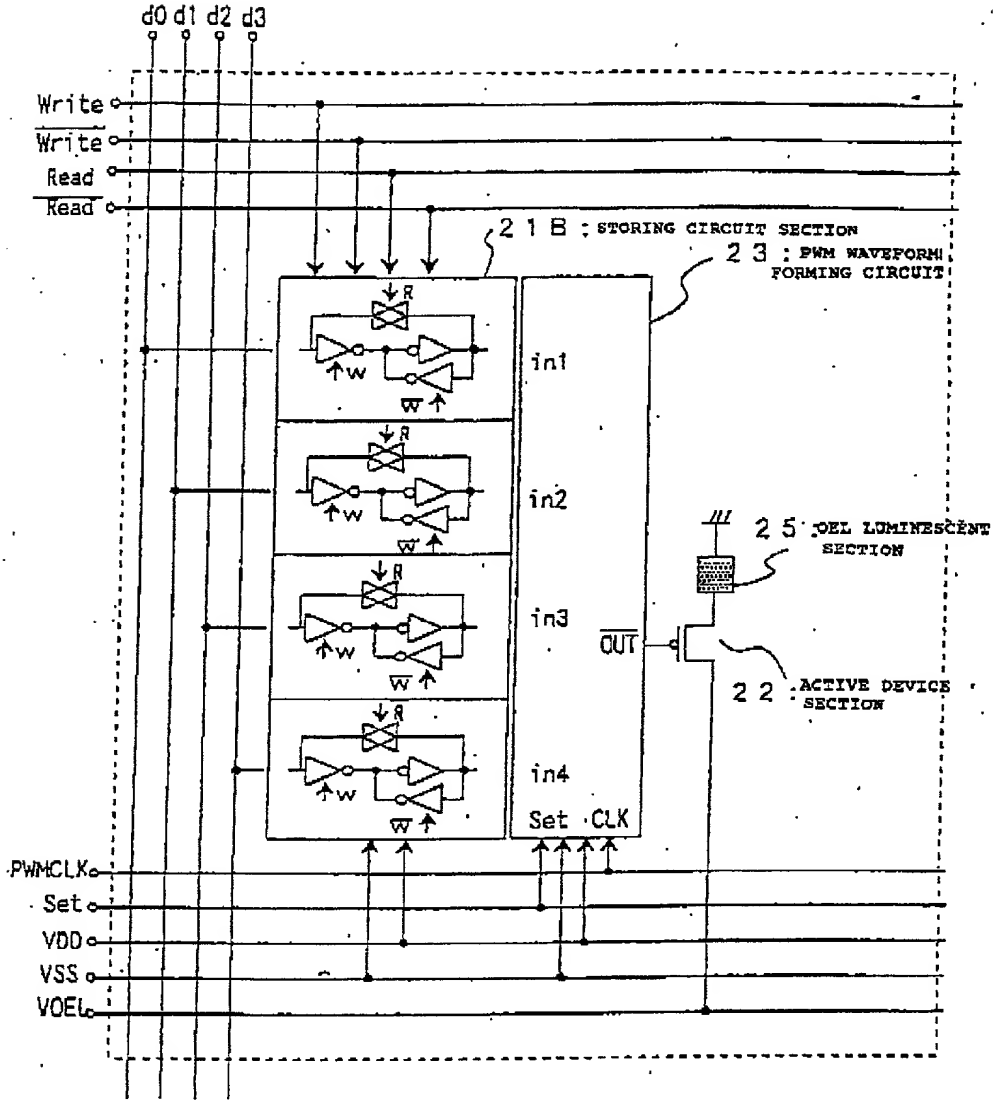
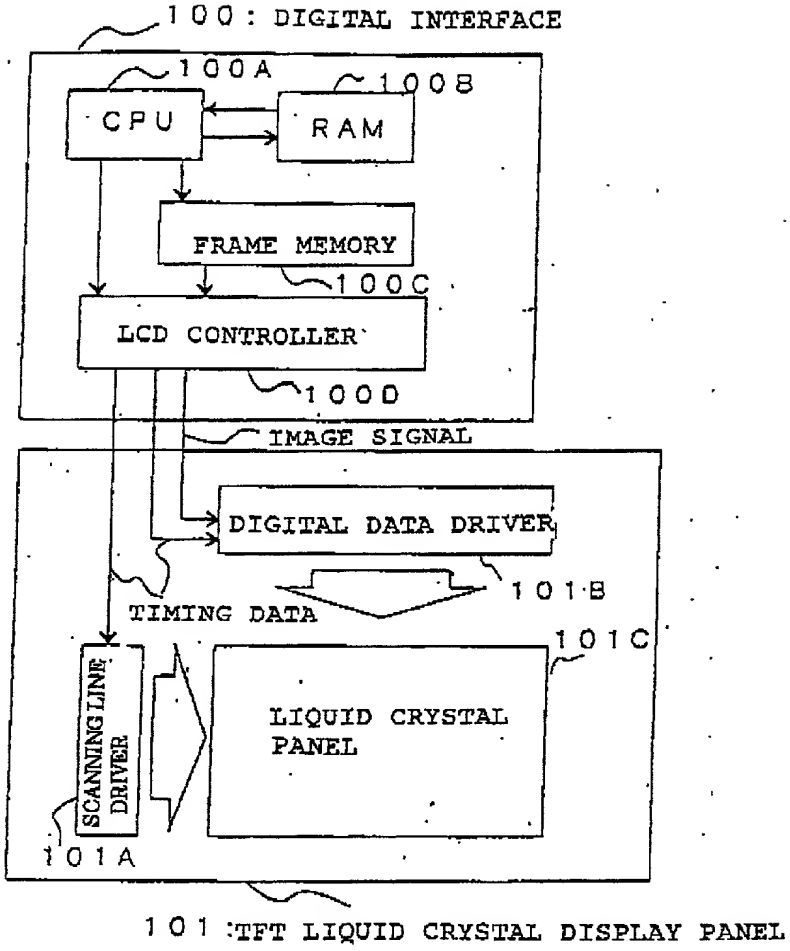

d0 d1 d2 d3
Write
Write
Read
Read
21B : STORING CIRCUIT SECTION
23 : PWM WAVEFORM FORMING CIRCUIT
R
W
in1
in2
in3
in4
Set
CLK
OUT
25 : OEL LUMINESCENT SECTION
22 : ACTIVE DEVICE SECTION
PWMCLK
Set
VDD
VSS
VOEL

Fig. 15


100 : DIGITAL INTERFACE
100A
100B
CPU
RAM
FRAME MEMORY
100C
LCD CONTROLLER
100D
IMAGE SIGNAL
DIGITAL DATA DRIVER
101B
TIMING DATA
101C
SCANNING LINE DRIVER
LIQUID CRYSTAL PANEL
101A
101 :TFT LIQUID CRYSTAL DISPLAY PANEL